

HD64941/2641

Asynchronous Communications Interface (ACI)

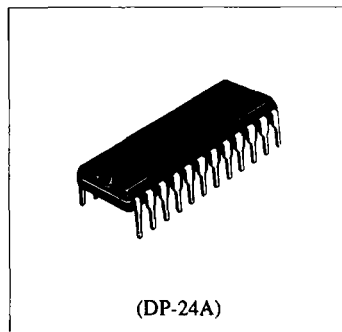
The HITACHI HD64941 is a universal asynchronous data communications controller chip that interfaces directly to most 8-bit microprocessors and may be used in a polled or interrupt-driven system environment. The HD64941 accepts programmed instructions from the microprocessor while supporting asynchronous serial data communications in full- or half-duplex mode.

The HD64941 serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

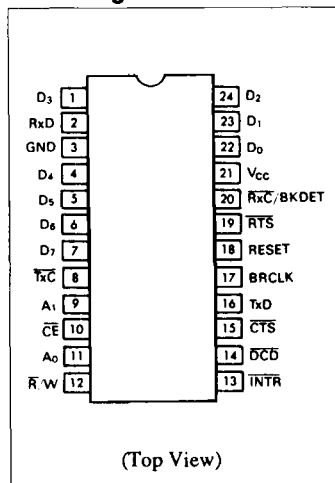
The HD64941 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

Features

- 5- to 8-bit characters plus parity
- 1, 1.5 or 2 stop bits transmitted
- Odd, even or no parity
- Parity, overrun and framing error detection
- Line break detection and generation
- False start bit detection
- Automatic serial echo mode (echoplex)
- Local or remote maintenance loopback mode
- Baud rate:
 - DC to 1 Mbps (1 x clock)
 - DC to 62.5 kbps (1 x clock)
 - DC to 15.625 kbps (64 x clock)
- Internal or external baud rate clock
- 16 internal rates
- Double-buffered transmitter and receiver
- Single +5 V power supply
- Pin-compatible with SCN2641 (Signetics)



Pin Arrangement



Ordering Information

Type No.	External Clock	Package
HD64941	3.6864 MHz	24-Pin
(Typ)		Plastic
		Skinny DIP

Please refer to the Data Sheet (No. ADE-202-002A) for the details.



Internal Block Diagram

The ACI consists of five major sections. These are the transmitter, receiver, timing, operation control and modem control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register.

Timing

The ACI contains a baud rate generator (BRG) which is programmable to accept external transmit or

receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for certain errors and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, appends start and stop bits, and, optionally, a parity bit, and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for two input signals and one output signal used for "handshaking" and status indication between the CPU and a modem.

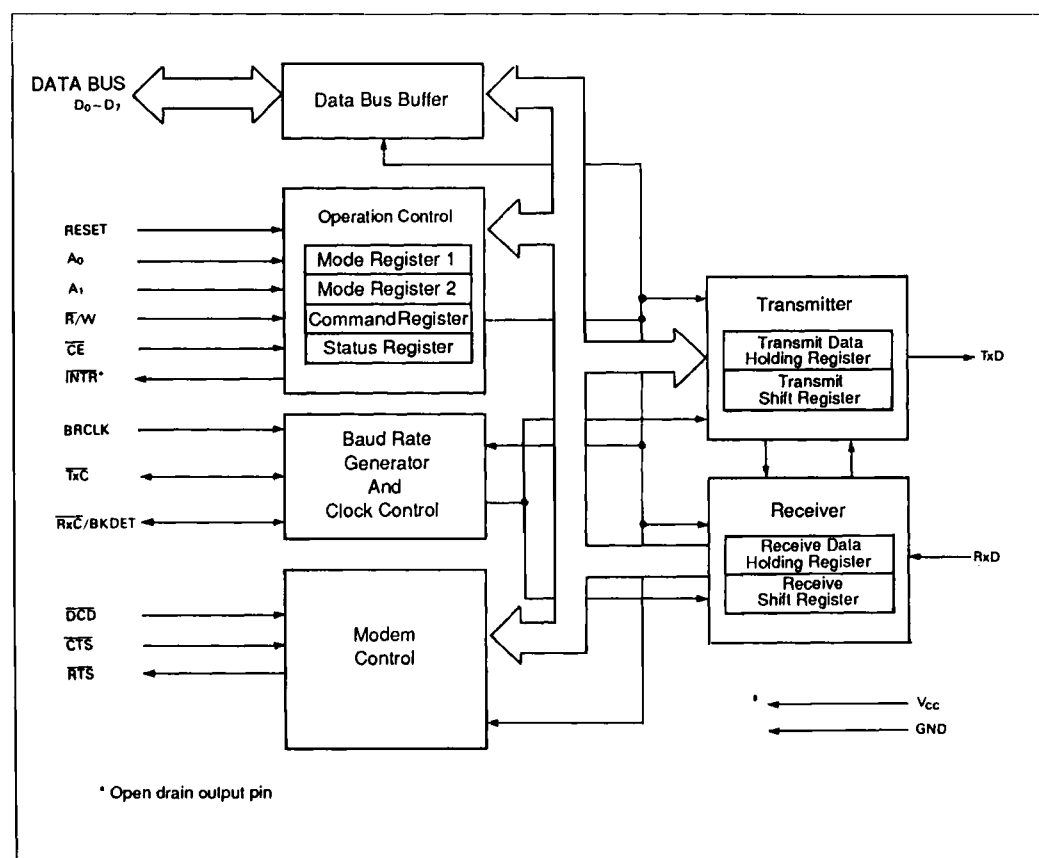


Figure 1. Internal Block Diagram

■ APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Serial peripherals

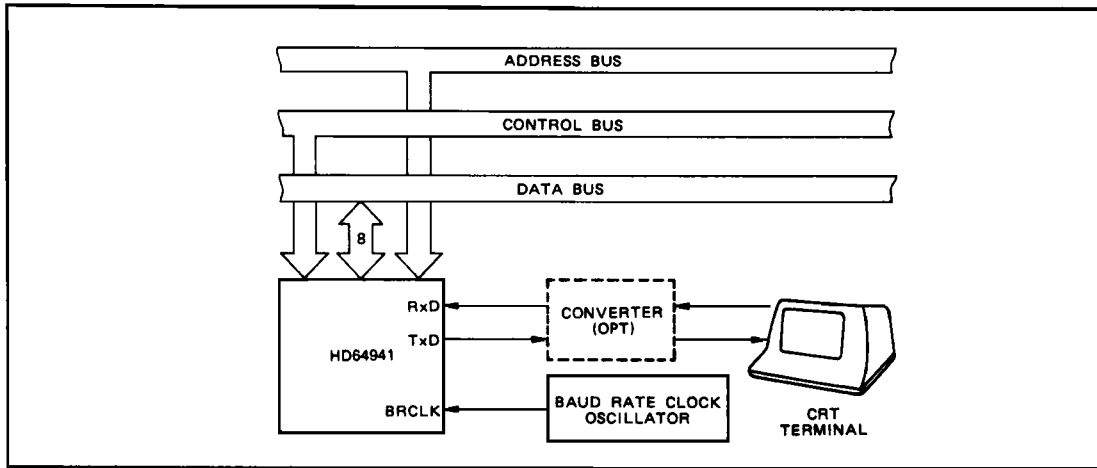


Figure 2 Asynchronous Interface to CRT Terminal

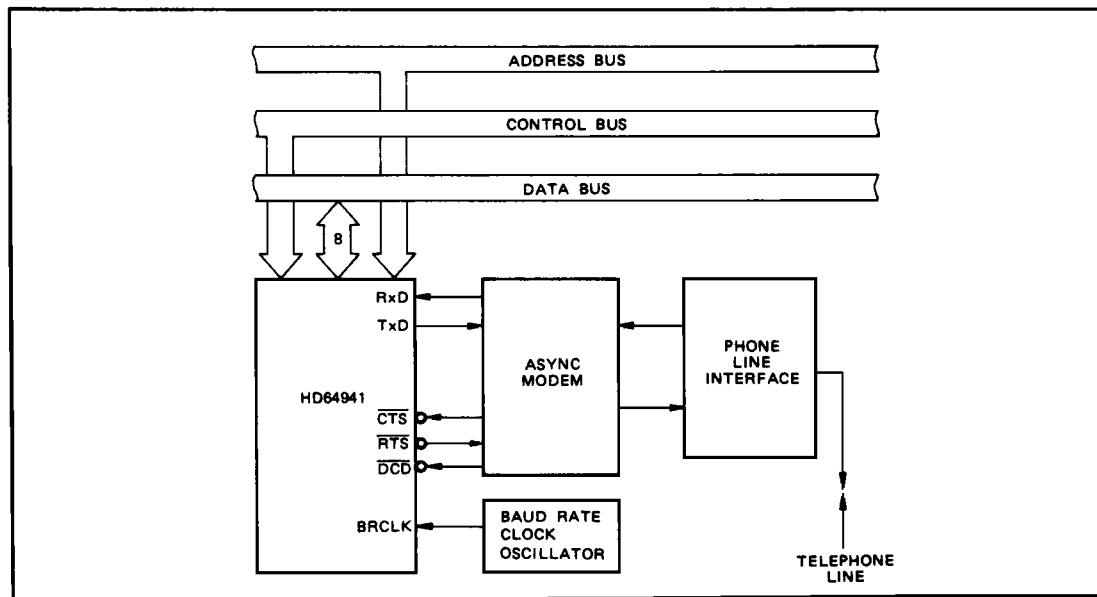


Figure 3 Asynchronous Interface to Telephone Lines